bladerRF - USB 3.0 Software Defined Radio

- (VC) TCXO + S6330
- DAC
- Narrower band baluns
- Chip selects for different endpoints?
- GPIO
- Analog TXIQ and RXIQ for probing/debug
- Baluns/filters go here.
- USB 5V@300mA
- 1.2V - SMPS max 3A 90% eff
- 3.58V - SMPS max 1.3A 95% eff
- 3.3V Analog 280mA/500mA - Linear LDO for LMS TX
- 3.3V Analog 220mA/500mA - Linear LDO for LMS RX
- 3.3V Digital 106mA/200mA - Linear LDO for LMS RX/TX
- 2.5V Analog 30mA/100mA - Linear LDO VCO/PLLs
- 1.8V Analog 100mA/200mA - Linear LDO for LMS
- 1.8V Digital 190mA/400mA - Linear LDO for signalling
**MSEL[3..0]**

- **VCCA_C4**: MSEL[3]
- **VCCA_C4**: MSEL[2]
- **VCCA_C4**: MSEL[1]
- **VCCA_C4**: MSEL[0]

**Notes**:
- MSEL pins should be connected directly to VCCA or GND.
- **C4 handbook pg 171**: MSEL[0..3] = "1100" @ 3.3/3.0/2.5V
- **C4 handbook pg 171**: PS-FAST = "1100" @ 3.3/3.0/2.5V
- **C4 handbook pg 171**: PS-STD = "0000" @ 3.3/3.0/2.5V
- **C4 handbook pg 171**: FPP-FAST = "1110" @ 1.8/1.5V
- **C4 handbook pg 171**: FPP-STD = "1111" @ 1.8/1.5V

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**JTAG is on BANK 1 aka VCCIO_L_C4**

**Config is on BANK 1 aka VCCIO_L_C4**
Avoid VREF pins due to their slow IO times. IC528 has to be a CTS pin. DATA[1..7] have to be from GPIF[0..15].

UDCLK has to be a CTL pin. DATA[0..7] have to be from GPIF[0..15].
Avoid VREF pins due to their slow IO times.
In 32-bit GPIF mode UART is (FX3 data pg 33):

- GPIO[55](C2) = UART_TX
- GPIO[56](D5) = UART_RX

UART_CS was added to allow the FPGA to use the MISO/MOSI lines to communicate via UART with the FX3. CS can also be deasserted to write to flash after boot.

FX3 datasheet pg 7:

- SPI+USB is primary, USB only should be achievable
- SPI+USB or failure - PMODE[2..0] = "011"
- USB boot - PMODE[2..0] = "111"

Add R257 so that SPI-boot works. C4's HIGH-Z state has a weak pull up, so it can be balanced out with a weak pull-down.
FX3 DEBUG + CLOCK SEL

DEBG TPs

FX3 JTAG

FSLC[2..0]

Debug LED

FPGA Version Resistor

XTAL / CLK

JTAG ICE CONNECT

FX3_I2C_SCL
FX3_I2C_SDA
CHARGER_DETECT

FX3 datasheet pg 8: 38.4MHz input CLK = FSLC[2:0] = "110"
USB CONNECTIONS

USB3.0 MICRO TYPE B

USB Positive Overvoltage Protection Controller

ESD DEVICE

PART_NUMBER = SP3010-04UTG
Manufacturer = Littlefuse

File Nuand
Sheet 8 of 14
Date Thursday, January 29, 2015

PART_NUMBER = NCP915NT1G
Manufacturer = ON Semiconductor
FX3 POWER

FX3 POWER

U3RX_VDDQ

AVDD

U3TX_VDDQ

CVDDQ

U3RX_VDDQ

VDD

VIO1
c

VIO2
c

VIO3
c

VIO4
c

VIO5
c

FPGA VCCIO

VIO1

VIO2

VIO3

VIO4

VIO5

U3RX_VDDQ = V1P2
U3TX_VDDQ = V1P2
AVDD = V1P2
CVDDQ = V1P8
VDD = V1P2
VIO1 = V1P8
VIO2 = V1P8
VIO3 = V1P8
VIO4 = V1P8
VIO5 = V1P8
PVDDVGG must be 3.3V

Analog 1.8V

Digital 1.8V

PVDDAD33 [A-D] are the ADC/DAC IO buf Vref pins

PVDDVGG must be 3.3V

PVDDSPI33 is a Vref for the SPI + PLLCLK. Pin 71, 74 need split plane

PLLCLK is Vref'd by PVDDSPI33

PVDD33 is further away from the other pins so parts are replicated

Analog 3.3V

Digital 3.3V

PVDDAD33 must be 3.3V

PVDDAD33 is a Vref for the SPI + PLLCLK. Pin 71, 74 need split plane

Analog 3.3V

Digital 3.3V

LMS digital
LMS ANALOG + RF

300MHz - 2.8GHz

1.5GHz - 3.8GHz

RF Shield tabs

LMS ANALOG + RF
These caps have to be close to their respective Vref pins.
POWER DISTRIBUTION

The idea is to drop to 1.2V and 3.58V with SMPS.
Then drop to 3.3, 2.5, 1.8 from the 3.58V SMPS.

1.2V  (min:200mA, typ:800mA) / 3100mA / 90% eff

Analog 3.3V  280mA / 500mA
Analog 3.3V  220mA / 500mA
Digital 3.3V  106mA / 200mA
Analog 1.8V  ~100mA / 200mA
Digital 1.8V  190mA / 400mA

3.58V  ~800mA / 1300mA / 95% eff

Analog 3.3V  220mA / 500mA
Digital 3.3V  106mA / 200mA

Digital 3.3V  106mA / 200mA
Digital 1.8V  190mA / 400mA

Analog 2.5V  30mA / 100mA
POWER SELECTION + DEBUG

Jumpered power selection
DC barrel vs USB3 bus

Scatter these testpoints throughout the design.
Testpoints will be PTH

C121 100uF_10V
C123 330uF_10V
C124 330uF_10V

TP39
PART_NUMBER = RAPC712X
Manufacturer = Switchcraft Inc.

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