MOUNTING HOLES - 80 mil holes
120 annular ring
To be placed in each corner of board

Scatter these testpoints throughout the design.
Testpoints will be PTH
AD9361 - 2x2 MIMO RF (47MHz - 6GHz)

3 GHz - 6 GHz

70 MHz - 3 GHz

47 MHz - 3 GHz

3 GHz - 6 GHz

70 MHz - 3 GHz

47 MHz - 3 GHz
FPPx8 / no compression / std. POR
MSEL[4:0] = 11000

Compatible with:
FPPx8 / compression / std. POR
MSEL[4:0] = 11010
Add R21 so that SPI-boot works. C5's HIGH-Z state has a weak pull up, so it can be balanced out with a weak pull-down.

FLASH VCC: 3.3V  
25 mA

FX3 datasheet pg 7:
SPI+USB is primary, USB only should be achievable
SPI+USB on failure - PMODE[2:0] = "0F1"
USB boot - PMODE[2:0] = "F11"

SPI Flash

Part Number = W25Q32JVSSIQ
Manufacturer = Winbond
FLASH VCC: 3.3V

Add R21 so that SPI-boot works. C5's HIGH-Z state has a weak pull up, so it can be balanced out with a weak pull-down.
FX3 DEBUG + CLOCK SEL

FX3 JTAG

FX3 datasheet pg 8:
38.4MHz input CLK - FSLC[2:0] = "110"

Title: FX3 JTAG
Part Number: M50-3601042
Manufacturer: Harwin
FX3 POWER

U3RX_VDDQ

AVDD

CVDDQ

VDD

VI01

VI02

VI03

VI04

VI05

FPGA VCCIO

U3RX_VDDQ = V1P2
U3TX_VDDQ = V1P2
AVDD = V1P2
CVDDQ = V1P8
VDD = V1P8
VI01 = V1P8
VI02 = V1P8
VI03 = V1P8
VI04 = V3P3
VI05 = V1P8

Changed C103 from 2.2uF to 4.7uF
POWER - 1.1V/1.8V/3.3V

Digital 1.1V 2000-4000mA / 4000mA

Digital 1.8V 1000mA / 4000mA

Digital 3.3V 512mA / 1000mA

VSENSE should be connected after the last output capacitor.
**POWER - 1.3V**

**Analog 1.3V 1050mA / 1200mA**

VOUT = 0.5 V * (1 + (R1 / R2))

**Digital 1.3V 1050mA / 1200mA**

VOUT = 0.5 V * (1 + (R1 / R2))

Place inductors inline with RF trace
Decoupling caps should be close
**POWER - 1.2V/2.5V**

**Digital 1.2V**  
197mA / 1200mA

\[ V_{OUT} = 0.5 \times (1 + \frac{R_1}{R_2}) \]

**Digital 2.5V**  
307mA / 1200mA

\[ V_{OUT} = 0.5 \times (1 + \frac{R_1}{R_2}) \]
POWER MUXES AND MONITOR

If DC barrel jack (VDC) is floating or does not provide at least 4 V, power mux will select USB VBUS.

### XB VCCIO SELECTION

<table>
<thead>
<tr>
<th>SEL2</th>
<th>SEL1</th>
<th>VCCIO / VCCPD</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>R1-2 / R1-2</td>
</tr>
<tr>
<td>3.3V</td>
<td>GND</td>
<td>1.8 V / 2.5 V</td>
</tr>
<tr>
<td>GND</td>
<td>3.3V</td>
<td>2.5 V / 2.5 V</td>
</tr>
<tr>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3 V / 3.3 V (DEFAULT)</td>
</tr>
</tbody>
</table>