CYCLONE V - CONFIGURATION

- CYCLONE V CONFIGURATION
- ROUTE TO AVOID AGGRESSORS
- FPPx8 / no compression / std. POR
  MSEL[4:0] = 11000
  Compatible with:
  FPPx8 / compression / std. POR
  MSEL[4:0] = 11010

Diagram showing configuration connections and settings.
USB CONNECTIONS

USB3.0 TYPE B

ESD DEVICE
FX3 POWER

VDD+AVDD 1.2V@200mA
U3VDDQ 1.8V@60mA

FX3 POWER

U3RX_VDDQ
AVDD
CVDDQ

U3TX_VDDQ

VDD

FPGA VCCIO

VI01 = V1P2
U3RX_VDDQ = V1P2
AVDD = V1P2
CVDDQ = V1P8
VDD = V1P8
VI01 = V1P8
VI02 = V1P8
VI03 = V1P8
VI04 = V3P3
VI05 = V1P8

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POWER - 1.3V

Analog 1.3V  1050mA / 1200mA

VOUT = 0.5 V * (1 + (R1 / R2))

Digital 1.3V  1050mA / 1200mA

VOUT = 0.5 V * (1 + (R1 / R2))
POWER - 1.2V/2.5V

Digital 1.2V   197mA / 1200mA

Digital 2.5V   307mA / 1200mA

VOUT = 0.5 V * (1 + (R1 / R2))
**POWER MUXES AND MONITOR**

If DC barrel jack (VDC) is floating or does not provide at least 4 V, power mux will select USB VBUS.

<table>
<thead>
<tr>
<th>SEL1</th>
<th>SEL2</th>
<th>VCCIO / VCCPD</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>3.3V / 1.8 V / 2.5 V</td>
</tr>
<tr>
<td>3.3V</td>
<td>GND</td>
<td>2.5 V / 2.5 V</td>
</tr>
<tr>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3 V / 3.3 V (DEFAULT)</td>
</tr>
</tbody>
</table>

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