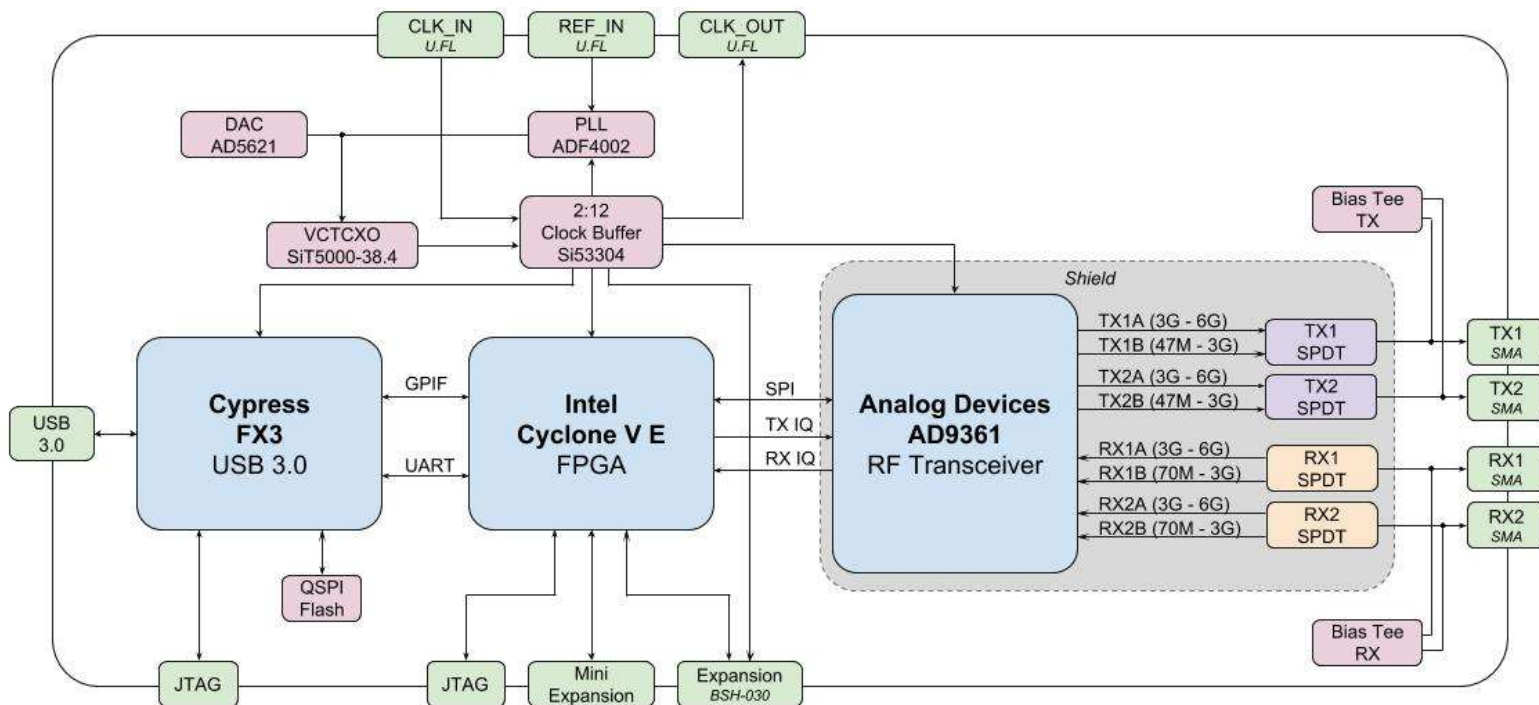
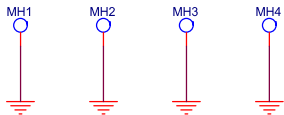


# bladerRF 2.0 micro - USB 3.0 Software Defined Radio



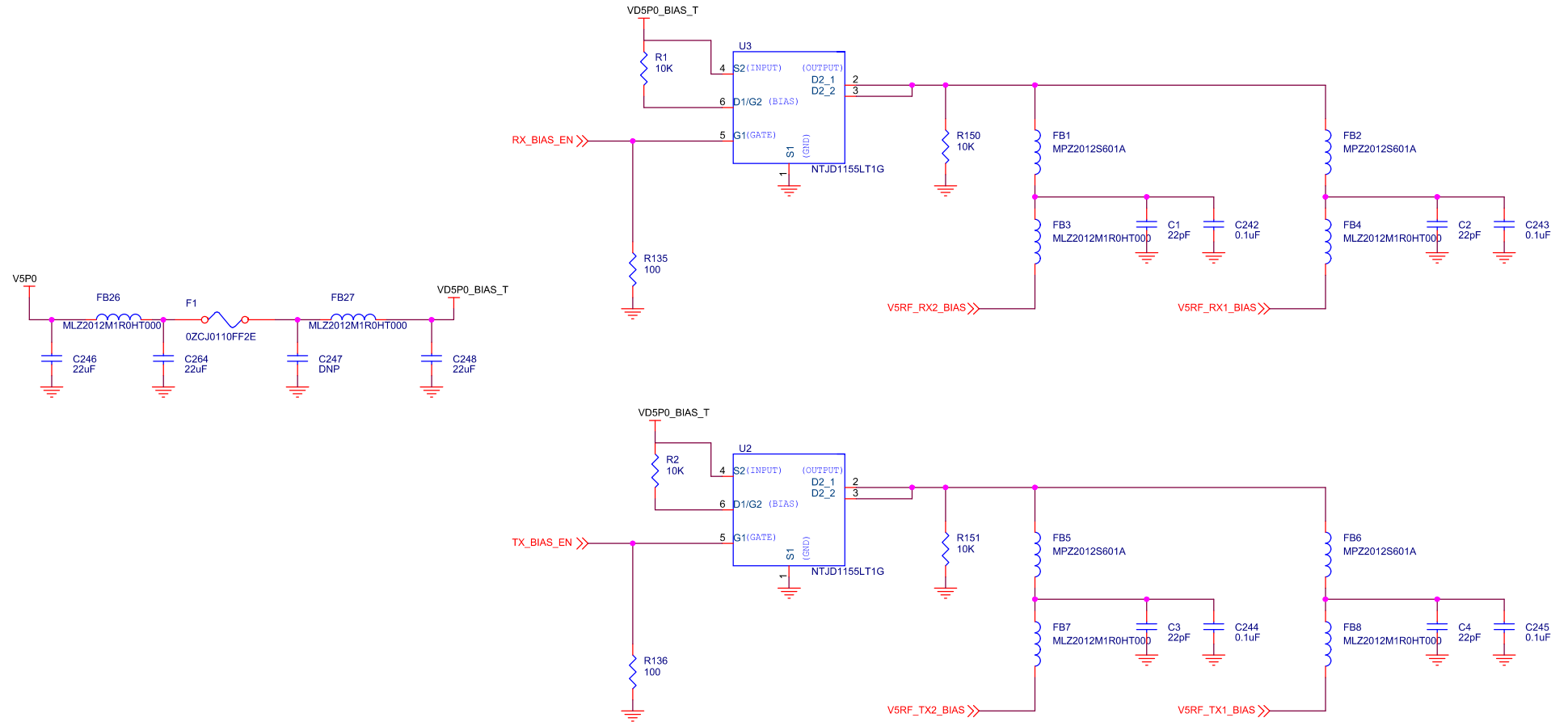
MOUNTING HOLES - 80 mil holes  
120 annular ring  
To be placed in each corner of board

Scatter these testpoints throughout the design.  
Testpoints will be PTH



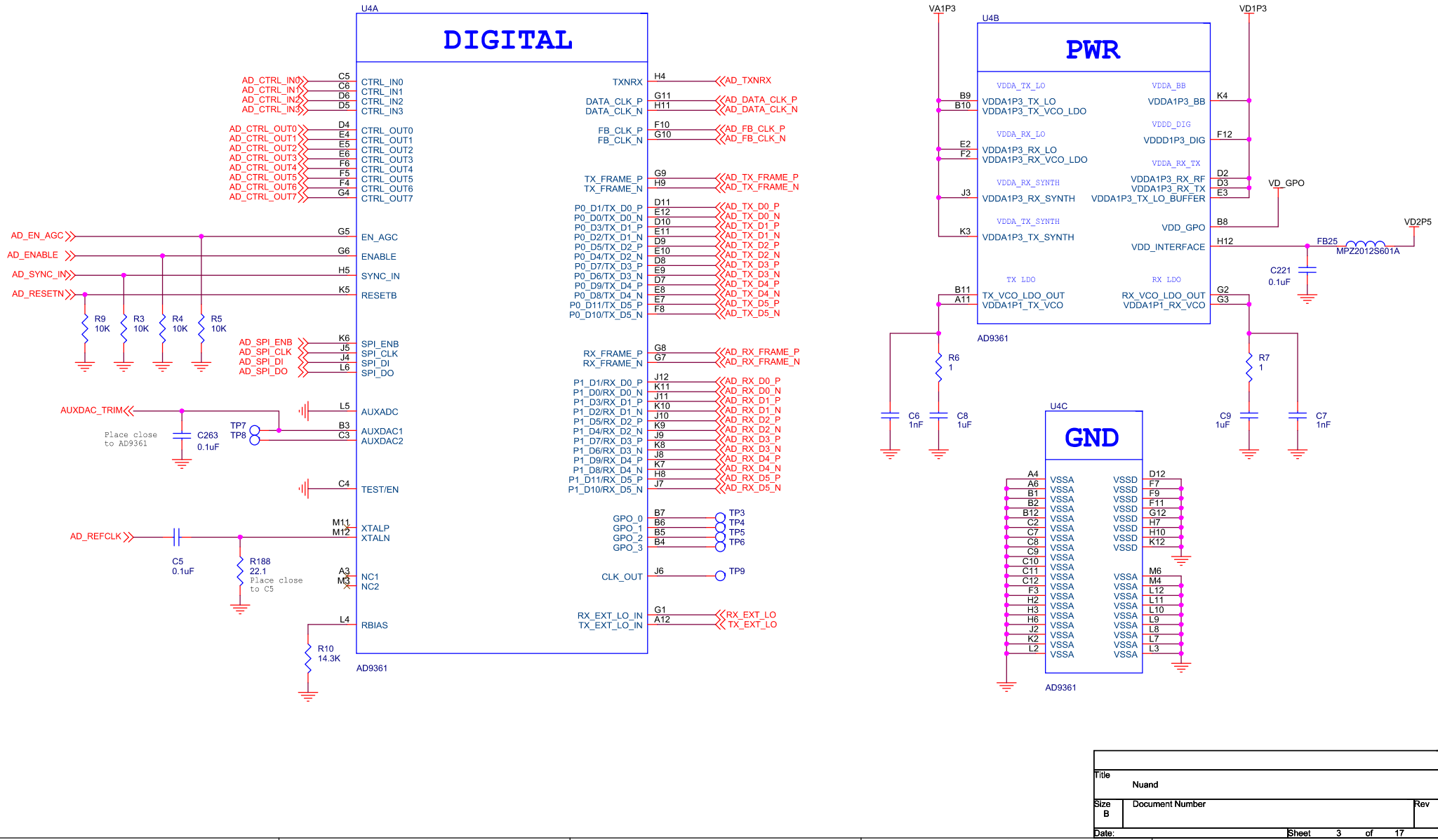
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Size	Document Number	Rev	
B		1.4	
Date:	Sheet 1 of 17		

# RF SMA BIAS TEE



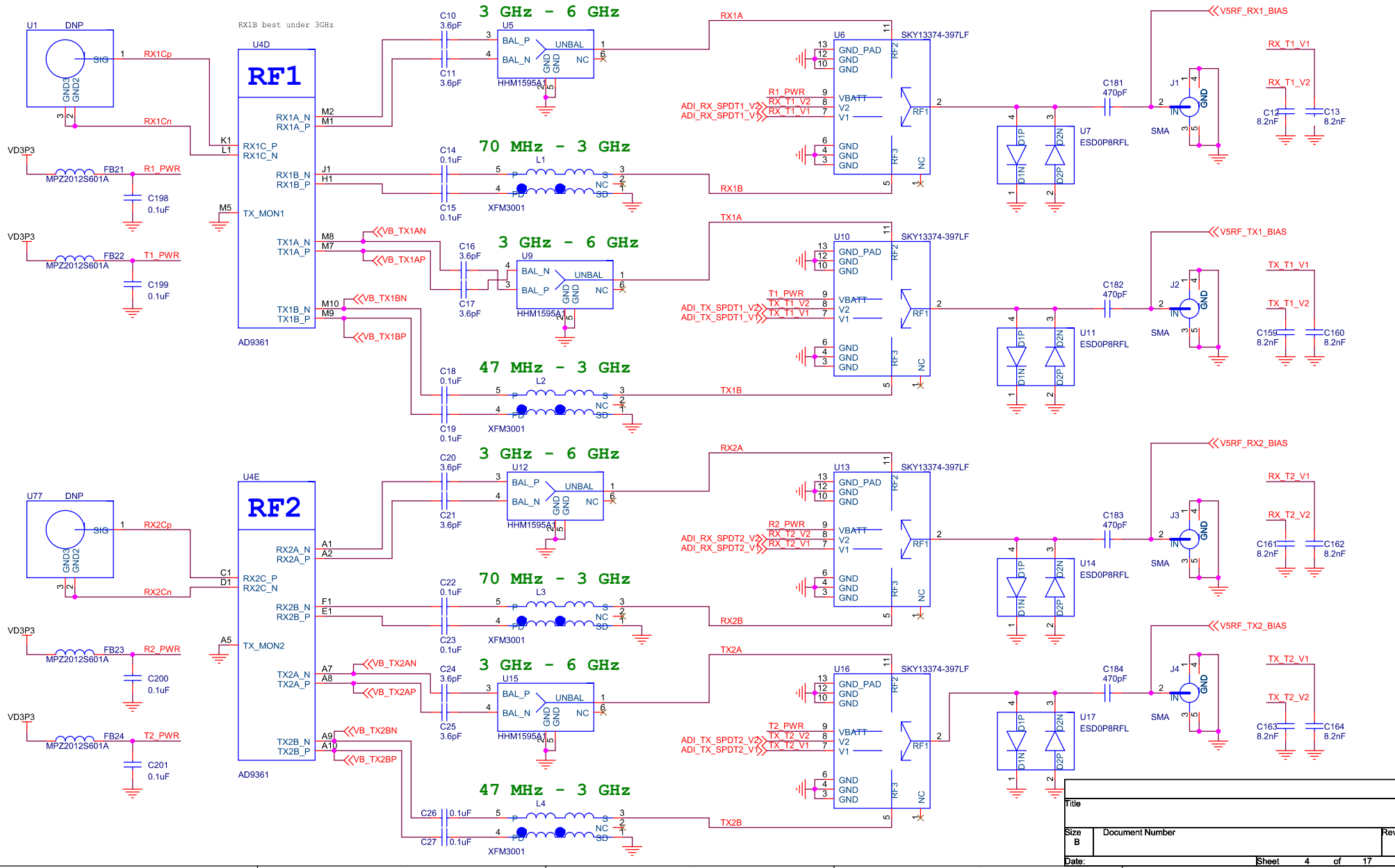
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Size	Document Number		Rev
Date:	Sheet 2 of 17		

# AD9361 - Digital



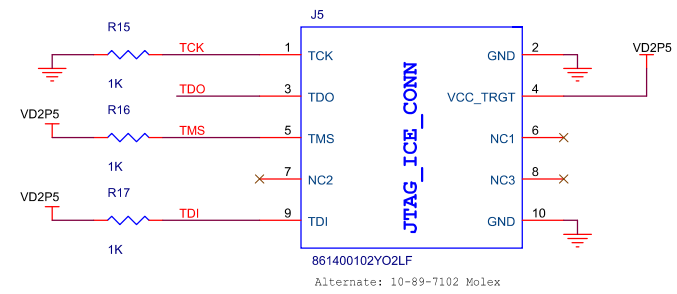
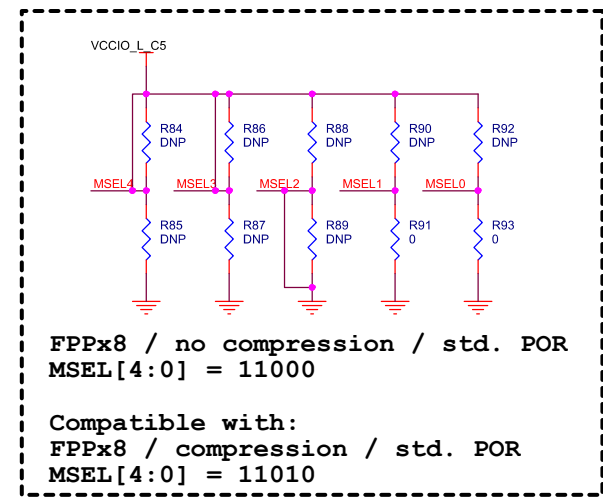
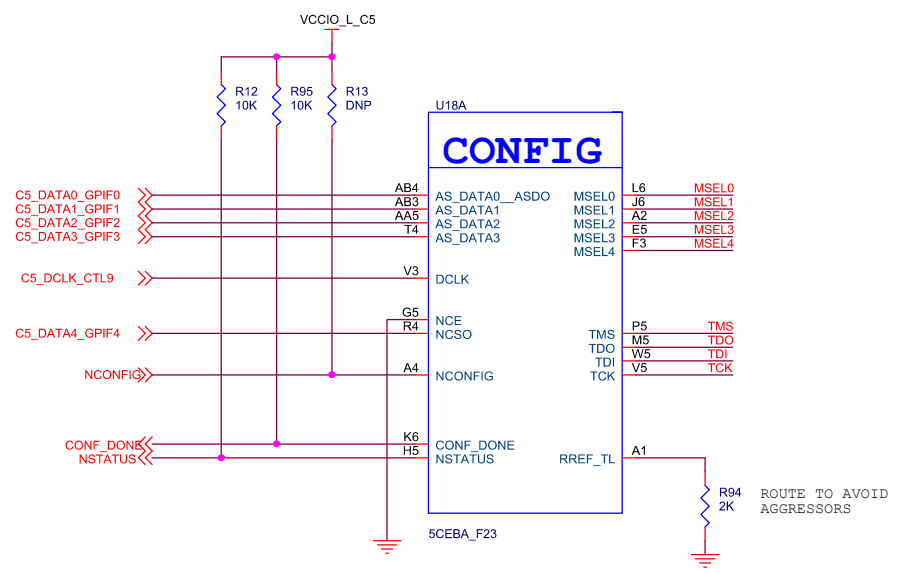
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Size	B	Document Number	Rev
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# AD9361 - 2x2 MIMO RF ( 47MHz - 6GHz )



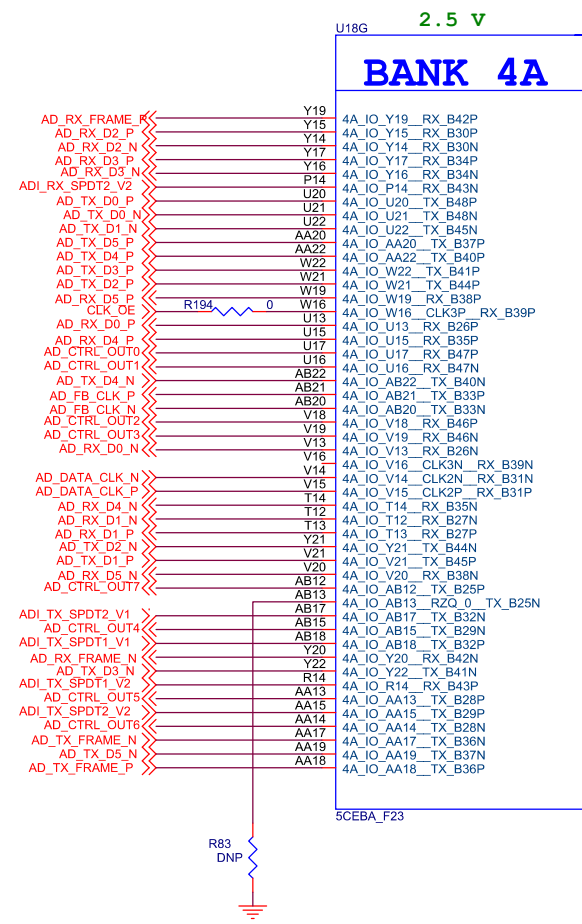
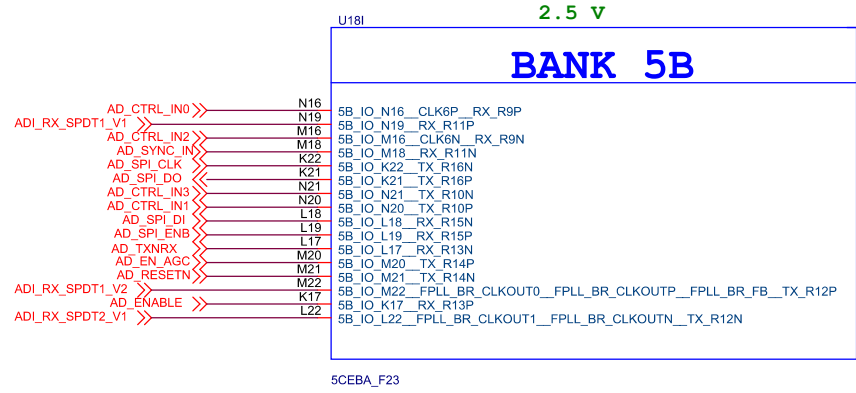
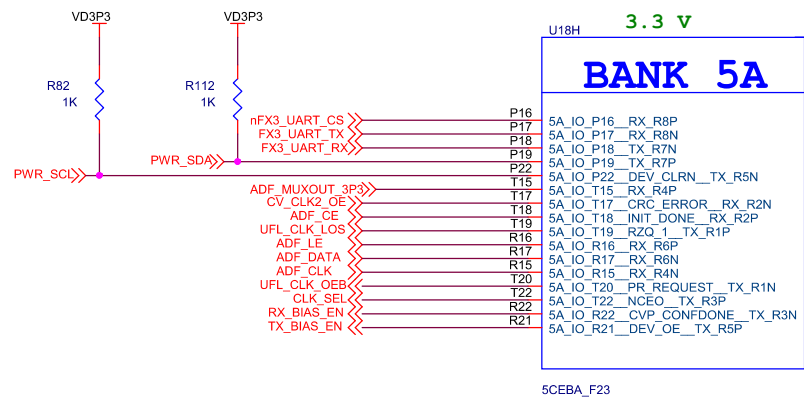
Title		
Size	Document Number	Rev
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# CYCLONE V - CONFIGURATION



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# CYCLONE V - BANKS 4A / 5A / 5B



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# CYCLONE V - BANKS 3A / 3B / 7A / 8A / EXPANSION

U18K **XB\_VCCIO (3.3 v / 2.5 v / 1.8 v)**

## BANK 8A

XB_GPIO13_E2F_6P	G6	8A_IO_G6_RX_T39P
XB_GPIO30_CLK_F2E_N	G8	8A_IO_G8_FPLL_TL_CLKOUT1_FPLL_TL_CLKOUTN_TX_T28N
XB_GPIO15_CLK_E2F_P	G10	8A_IO_G10_CLK9P_RX_T25P
XB_GPIO29_F2E_6P	F7	8A_IO_F7_TX_T40P
XB_GPIO6_E2F_3N	F9	8A_IO_F9_CLK8N_FPLL_TL_FBN_RX_T33N
XB_GPIO17_F2E_0P	L7	8A_IO_L7_TX_T26P
XB_GPIO11_E2F_5P	E9	8A_IO_E9_RX_T37P
XB_GPIO28_F2E_6N	E7	8A_IO_E7_TX_T40N
XB_GPIO14_CLK_E2F_N	F10	8A_IO_F10_CLK9N_RX_T25N
XB_GPIO16_F2E_0N	K7	8A_IO_K7_TX_T26N
XB_GPIO27_F2E_3P	E7	8A_IO_E7_TX_T40N
XB_GPIO10_E2F_5N	D9	8A_IO_E10_CLK8P_FPLL_TL_FBP_RX_T33P
XB_GPIO24_F2E_4N	D6	8A_IO_D9_RX_T37N
XB_GPIO27_F2E_5P	D7	8A_IO_D6_TX_T36N
XB_GPIO0_E2F_0N	J8	8A_IO_D7_TX_T38P
XB_GPIO3_E2F_1P	J9	8A_IO_J8_RX_T27N
XB_GPIO1_E2F_0P	J7	8A_IO_J7_RX_T27P
XB_GPIO4_E2F_2N	C9	8A_IO_C9_RX_T31N
XB_GPIO26_F2E_5N	C8	8A_IO_C8_TX_T38N
XB_GPIO25_F2E_4P	C6	8A_IO_C6_TX_T36P
XB_GPIO20_F2E_2N	B5	8A_IO_B5_TX_T32N
XB_GPIO23_F2E_3P	B6	8A_IO_B6_TX_T34P
XB_GPIO22_F2E_3N	B7	8A_IO_B7_TX_T34N
XB_GPIO31_CLK_F2E_P	H8	8A_IO_H8_FPLL_TL_CLKOUT0_FPLL_TL_CLKOUTP_FPLL_TL_FB_TX_T28P
XB_GPIO2_E2F_1N	H9	8A_IO_H9_RX_T29N
XB_GPIO12_E2F_8N	H6	8A_IO_H6_RX_T39N
XB_GPIO5_E2F_2P	A10	8A_IO_B10_RX_T31P
XB_GPIO19_F2E_1P	A10	8A_IO_A10_TX_T30P
XB_GPIO21_F2E_2P	A5	8A_IO_A5_TX_T32P
XB_GPIO8_E2F_4N	A7	8A_IO_A7_RX_T35N
XB_GPIO18_F2E_1N	A9	8A_IO_A8_TX_T35P
XB_GPIO9_E2F_4P	A8	8A_IO_A8_RX_T35P

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U18F **1.8 v**

## BANK 3B

FX3_CTL11	Y11	3B_IO_Y11_TX_B24N
GPIF31	Y10	3B_IO_Y10_TX_B17N
GPIF29	M9	3B_IO_M9_CLK0P_FPLL_BL_FBP_RX_B15P
GPIF27	M8	3B_IO_M8_CLK0N_FPLL_BL_FBN_RX_B15N
FX3_CTL5	F12	3B_IO_P12_TX_B20P
C5_DATA1_GPIF1	AB5	3B_IO_AB5_TX_B9P
C5_DATA0_GPIF0	AB7	3B_IO_AB6_TX_B9N
GPIF22	AB8	3B_IO_AB7_TX_B12P
GPIF25	Y9	3B_IO_AB8_TX_B13P
FX3_CTL0	R9	3B_IO_Y9_TX_B17P
FX3_CTL1	U12	3B_IO_R9_RX_B18P
FX3_CTL4	U11	3B_IO_U12_RX_B19P
FX3_CTL2	U10	3B_IO_U11_RX_B19N
GPIF26	V10	3B_IO_U10_RX_B14P
GPIF19	AA7	3B_IO_V10_RX_B10P
C5_DATA2_GPIF2	T10	3B_IO_AA7_TX_B12N
GPIF20	P8	3B_IO_T10_RX_B18N
FX3_CTL10	P9	3B_IO_P8_RX_B11N
FX3_CTL6	AB10	3B_IO_P9_CLK1N_RX_B23N
FX3_CTL8	AB11	3B_IO_AB10_FPLL_BL_CLKOUT1_FPLL_BL_CLKOUTN_TX_B21N
FX3_CTL7	V9	3B_IO_AB11_FPLL_BL_CLKOUT0_FPLL_BL_CLKOUTP_FPLL_BL_FB_TX_B21P
GPIF18	R12	3B_IO_V9_RX_B10N
FX3_CTL3	R10	3B_IO_R12_TX_B20N
FX3_CTL7	R11	3B_IO_R10_RX_B22N
PWR_STAT1	R11	3B_IO_R11_RX_B22P
GPIF21	N8	3B_IO_N8_RX_B11P
FX3_PCLK	N9	3B_IO_N9_CLK1P_RX_B23P
GPIF28	AA10	3B_IO_AA10_TX_B16N
FX3_CTL12	T9	3B_IO_AA12_TX_B24P
GPIF24	AA9	3B_IO_T9_RX_B14N
GPIF30	AA8	3B_IO_AA9_TX_B16N
GPIF23	AA8	3B_IO_AA8_TX_B13N

5CEBA\_F23

U18J **XB\_VCCIO (3.3 v / 2.5 v / 1.8 v)**

## BANK 7A

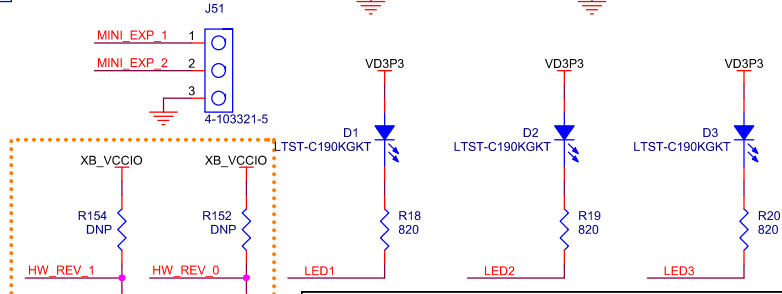
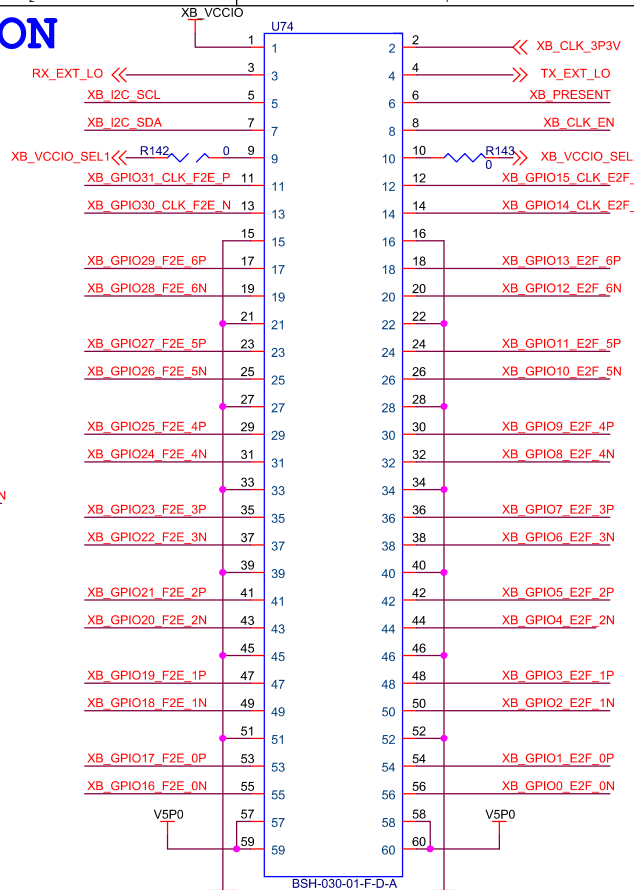
H18	7A_IO_H18_RX_T5N
H10	7A_IO_H10_TX_T16N
H11	7A_IO_H11_RX_T21P
H13	7A_IO_H13_CLK10P_RX_T17P
H14	7A_IO_H14_RX_T13P
H15	7A_IO_H14_RX_T13P
H16	7A_IO_H15_CLK11N_RX_T9N
G18	7A_IO_H16_CLK11P_RX_T9P
G17	7A_IO_G17_TX_T6P
G16	7A_IO_G16_TX_T4N
G15	7A_IO_G15_TX_T12P
G13	7A_IO_G13_CLK10N_RX_T17N
G12	7A_IO_G12_RX_T21N
G11	7A_IO_G11_TX_T18P
L8	7A_IO_L8_TX_T22P
F12	7A_IO_F12_TX_T18N
F13	7A_IO_F13_RX_T15N
F14	7A_IO_F14_TX_T12N
F15	7A_IO_F15_RX_T7N
K9	7A_IO_K9_TX_T22N
E12	7A_IO_E12_RX_T23N
E15	7A_IO_E15_RX_T22P
E14	7A_IO_E14_RX_T15P
E16	7A_IO_E16_RX_T3N
K20	7A_IO_K20_RX_T11P
D17	7A_IO_D17_RX_T3P
K16	7A_IO_K16_TX_T10N
K19	7A_IO_K19_RX_T11N
C13	7A_IO_C13_RX_T19N
C11	7A_IO_C11_TX_T24P
C16	7A_IO_C16_TX_T12N
C15	7A_IO_C15_RX_T11P
D12	7A_IO_D12_RX_T23P
D13	7A_IO_D13_RX_T19P
B16	7A_IO_B16_TX_T2P
B15	7A_IO_B15_RX_T11N
B12	7A_IO_B12_TX_T20P
B13	7A_IO_B13_TX_T14P
B11	7A_IO_B11_RZQ_2_TX_T24N
J18	7A_IO_J18_TX_T6N
J19	7A_IO_J19_TX_T6P
J17	7A_IO_J17_TX_T10P
J15	7A_IO_J13_RX_T13N
J11	7A_IO_J11_TX_T16P
A15	7A_IO_A15_TX_T8P
A14	7A_IO_A14_TX_T8N
A13	7A_IO_A13_TX_T14N
A12	7A_IO_A12_TX_T20N

U18E **1.8 v**

## BANK 3A

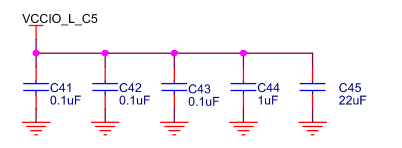
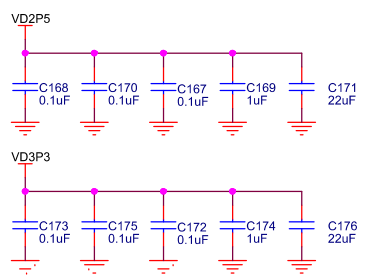
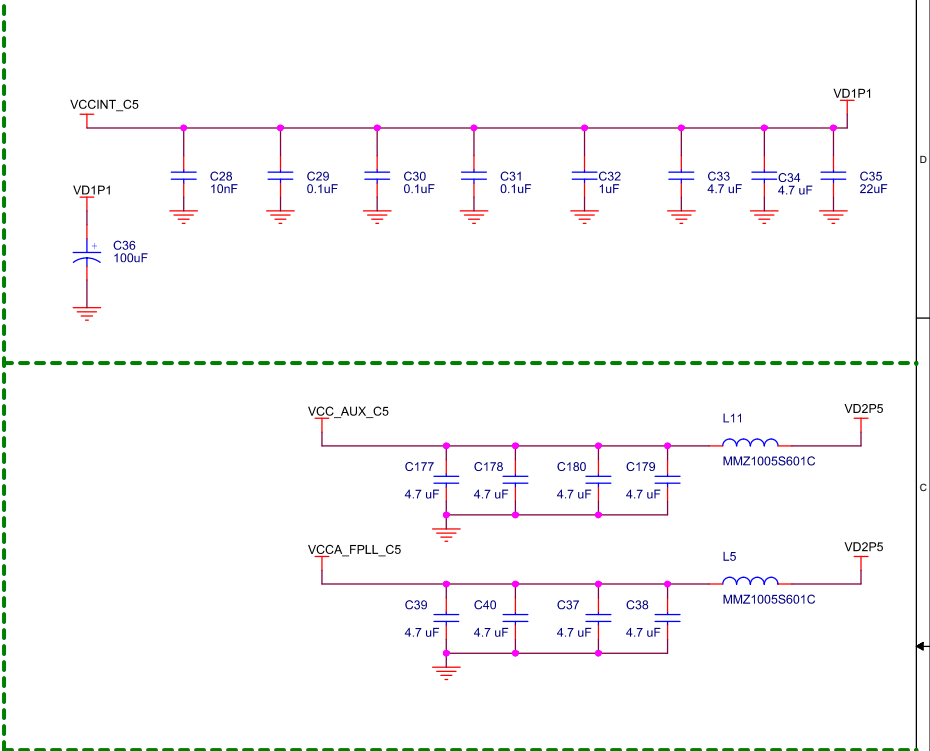
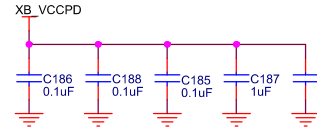
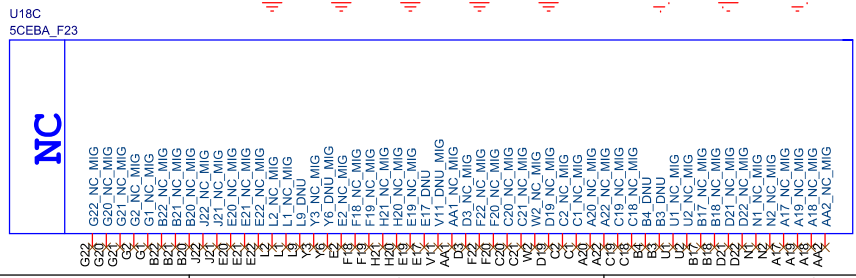
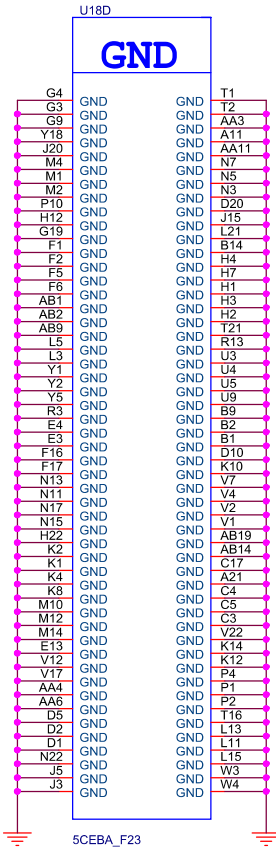
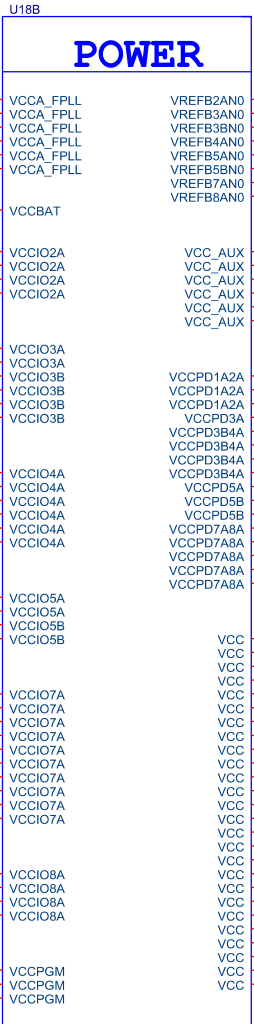
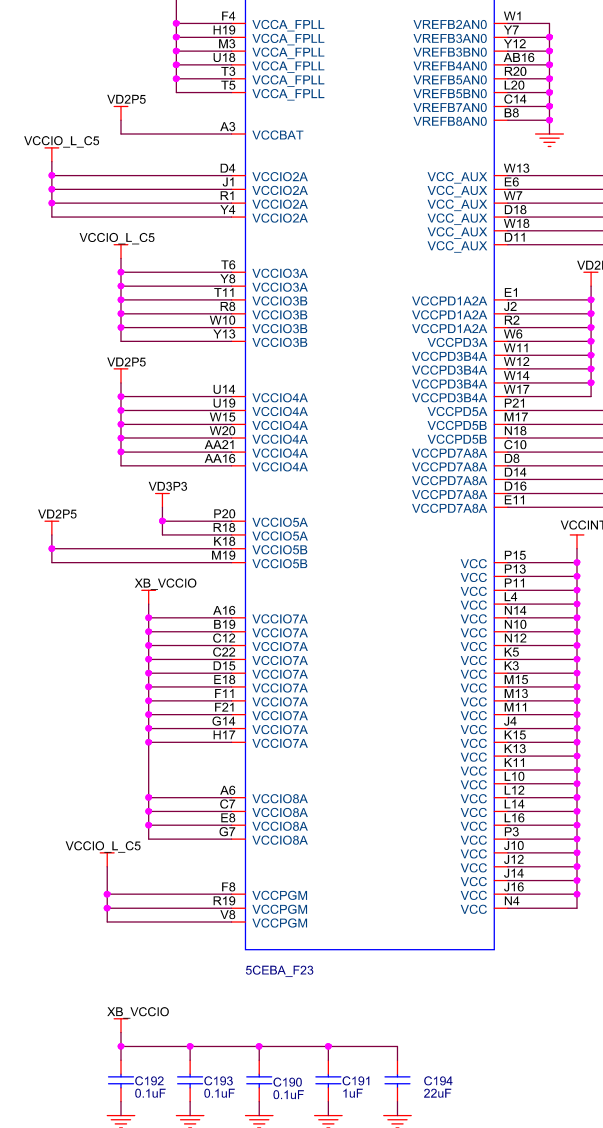
M7	3A_IO_M7_PR_ERROR_RX_B7P
GPIF15	3A_IO_M6_PR_DONE_RX_B7N
R5	3A_IO_R5_DATA8_RX_B1P
GPIF8	3A_IO_R6_DATA6_RX_B1N
R6	3A_IO_R7_PR_READY_TX_B8N
GPIF6	3A_IO_W9_DATA11_TX_B4P
W9	3A_IO_W8_DATA9_TX_B4N
GPIF11	3A_IO_R6_DATA10_RX_B3N
GPIF16	3A_IO_P7_TX_B8P
GPIF9	3A_IO_V6_DATA15_TX_B6P
W8	3A_IO_U8_DATA7_TX_B2P
P6	3A_IO_U7_DATA5_TX_B2N
GPIF14	3A_IO_U6_DATA13_TX_B6N
V6	3A_IO_N6_DATA12_RX_B3P
GPIF7	3A_IO_T8_CLKUSR_RX_B5P
GPIF5	3A_IO_T7_DATA14_RX_B5N
U7	
U6	
GPIF3	
N6	
T8	
GPIF10	
GPIF13	
T7	

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### POWER

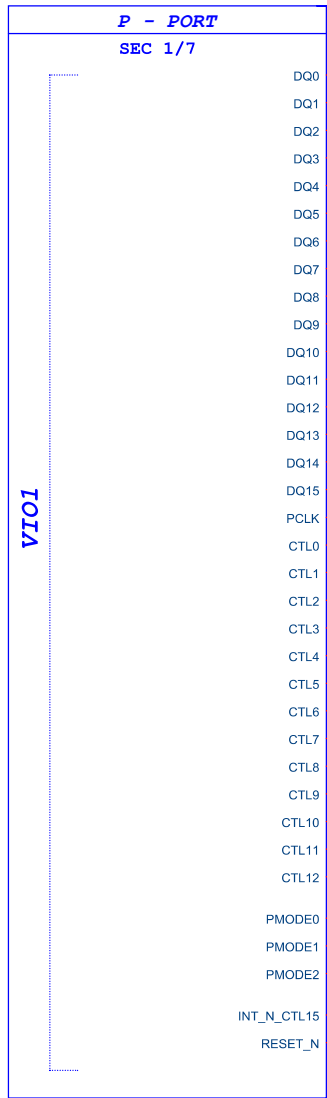


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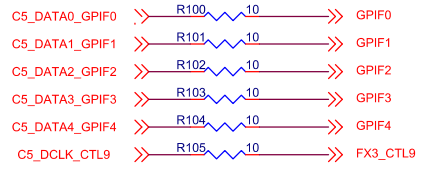


# FX3 GPIF + BOOT

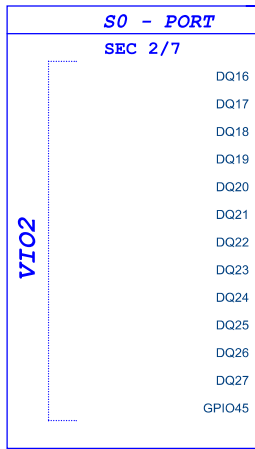
U19A



FX3

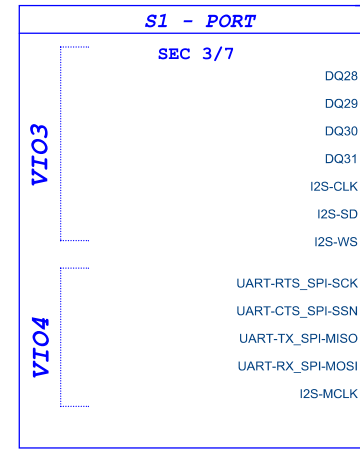


U19B



FX3

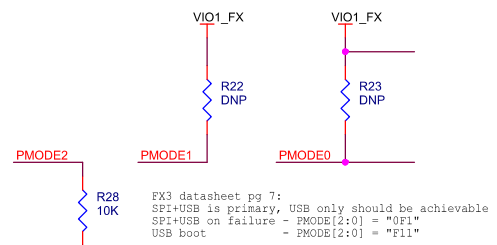
U19C



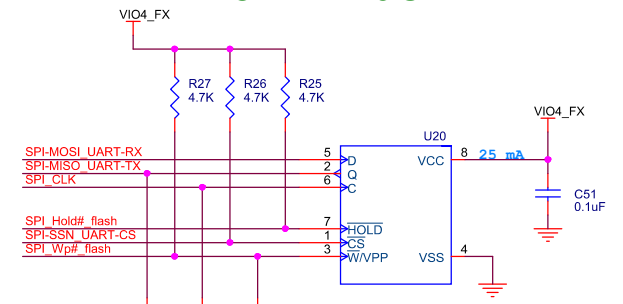
FX3

In 32-bit GPIF mode UART is (FX3 data pg 33):  
 GPIO[55](C2)=UART\_TX  
 GPIO[55](C2)=UART\_TX  
 GPIO[56](D5)=UART\_RX  
 UART\_CS was added to allow the FPGA to use the  
 MISO/MOSI lines to communicate via UART with the FX3.  
 CS can also be deasserted to write to flash after boot.

## PMODE[2..0]



## SPI Flash



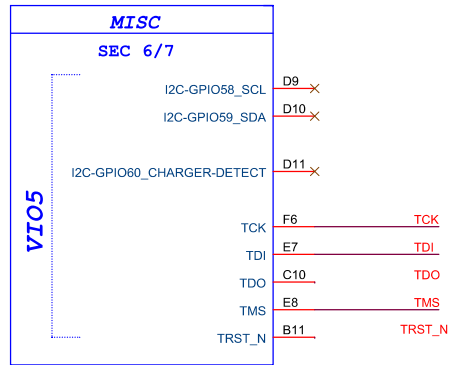
Add R21 so that SPI-boot works. C5's HIGH-Z state has a weak pull up, so it can be balanced out with a weak pull-down.



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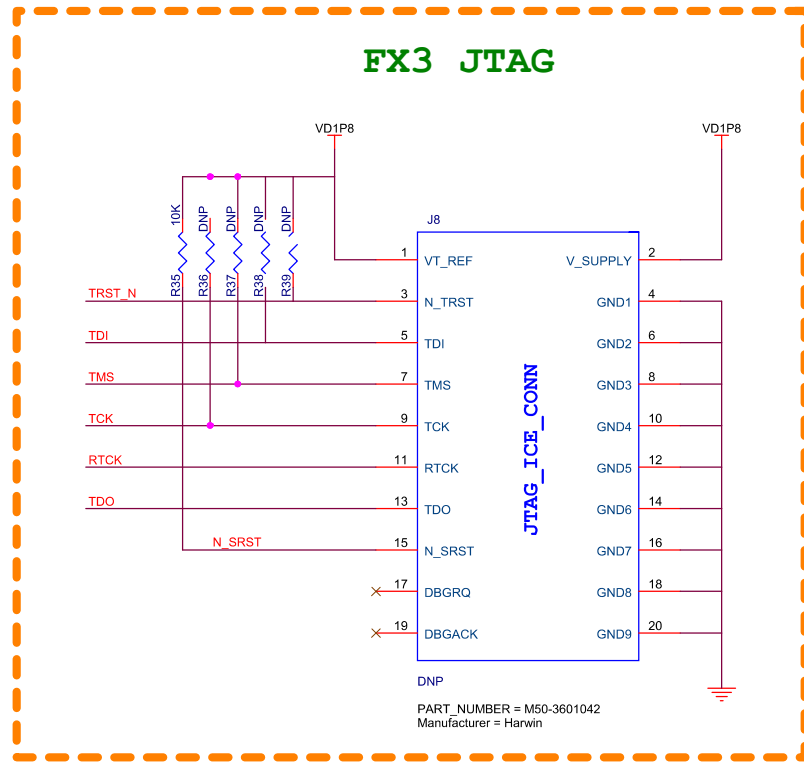
# FX3 DEBUG + CLOCK SEL

U19F



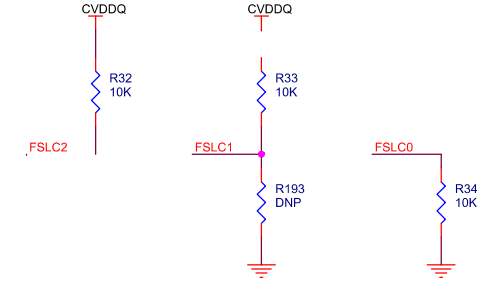
FX3

## FX3 JTAG

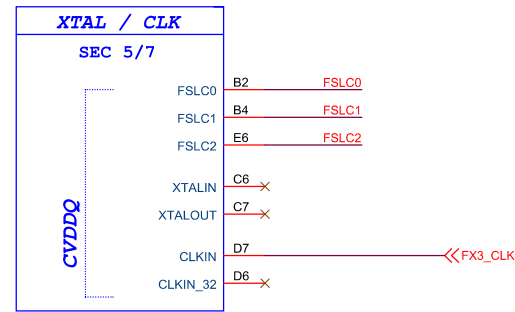


## FSLC[2..0]

FX3 datasheet pg 8:  
38.4MHz Input CLK = FSLC[2:0] = "110"



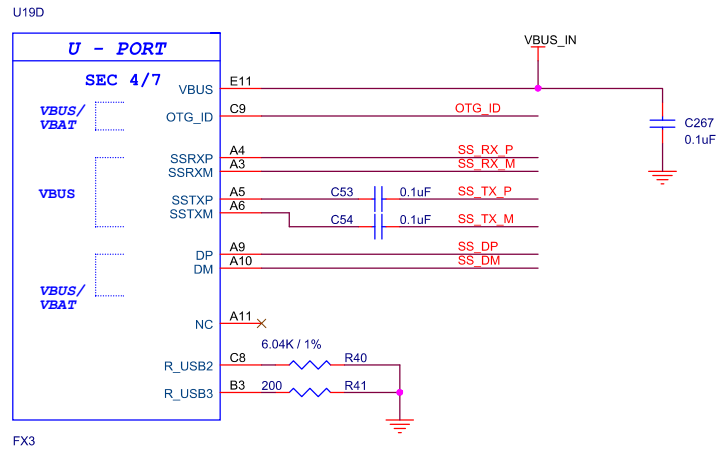
U19E



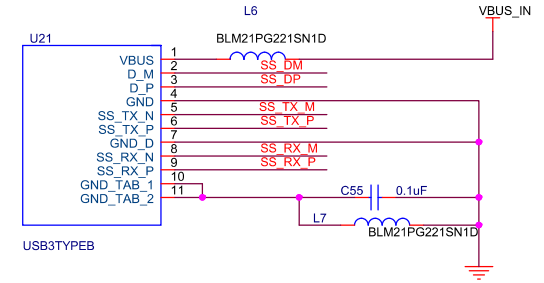
FX3

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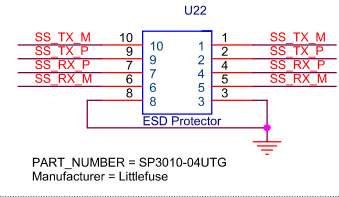
# USB CONNECTIONS



## USB3.0 TYPE B



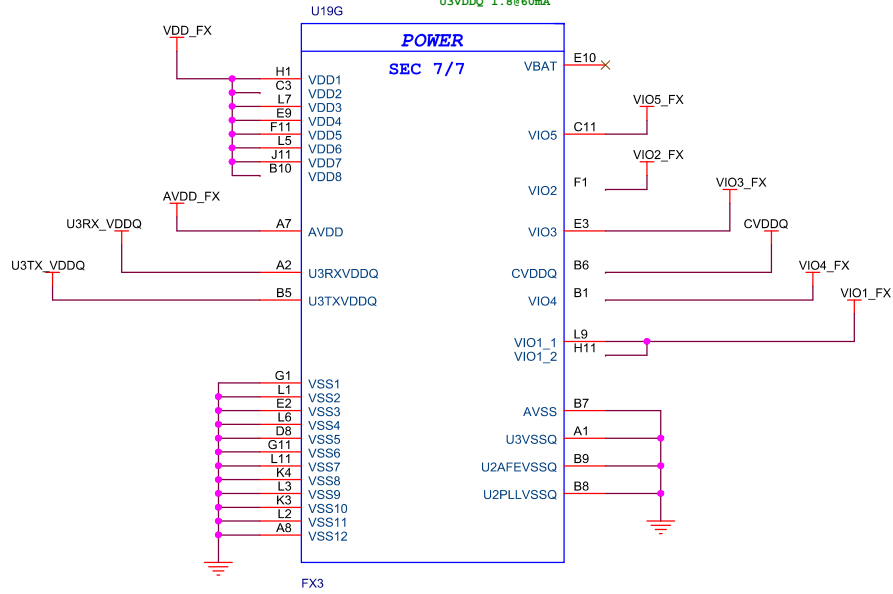
## ESD DEVICE



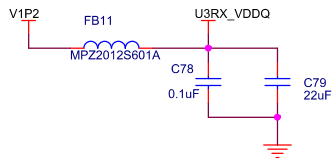
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# FX3 POWER

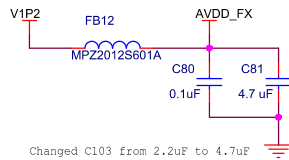
VDD+AVDD 1.2V@200mA  
U3VDDQ 1.8@60mA



## U3RX\_VDDQ

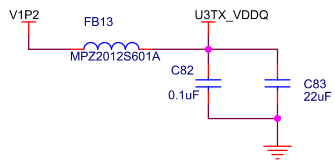


## AVDD

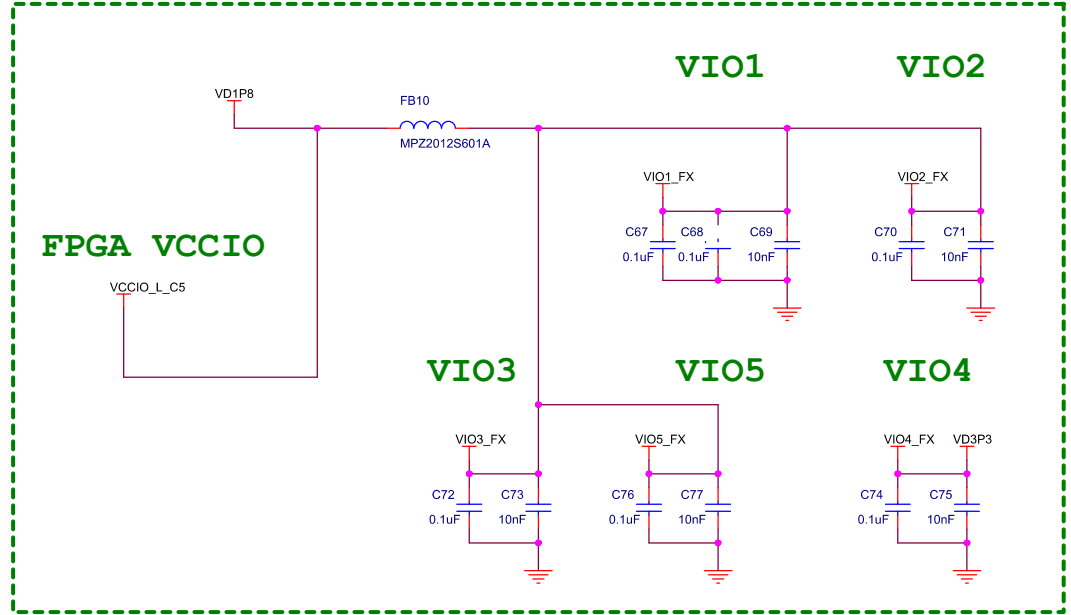
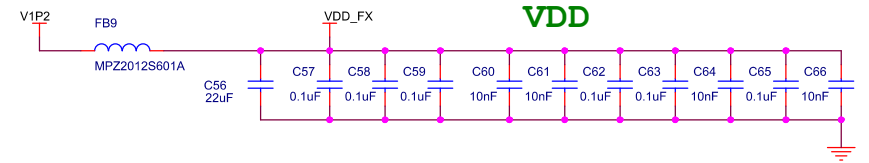
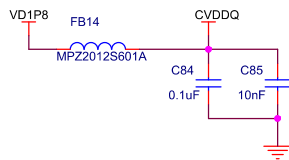


Changed C103 from 2.2uF to 4.7uF

## U3TX\_VDDQ



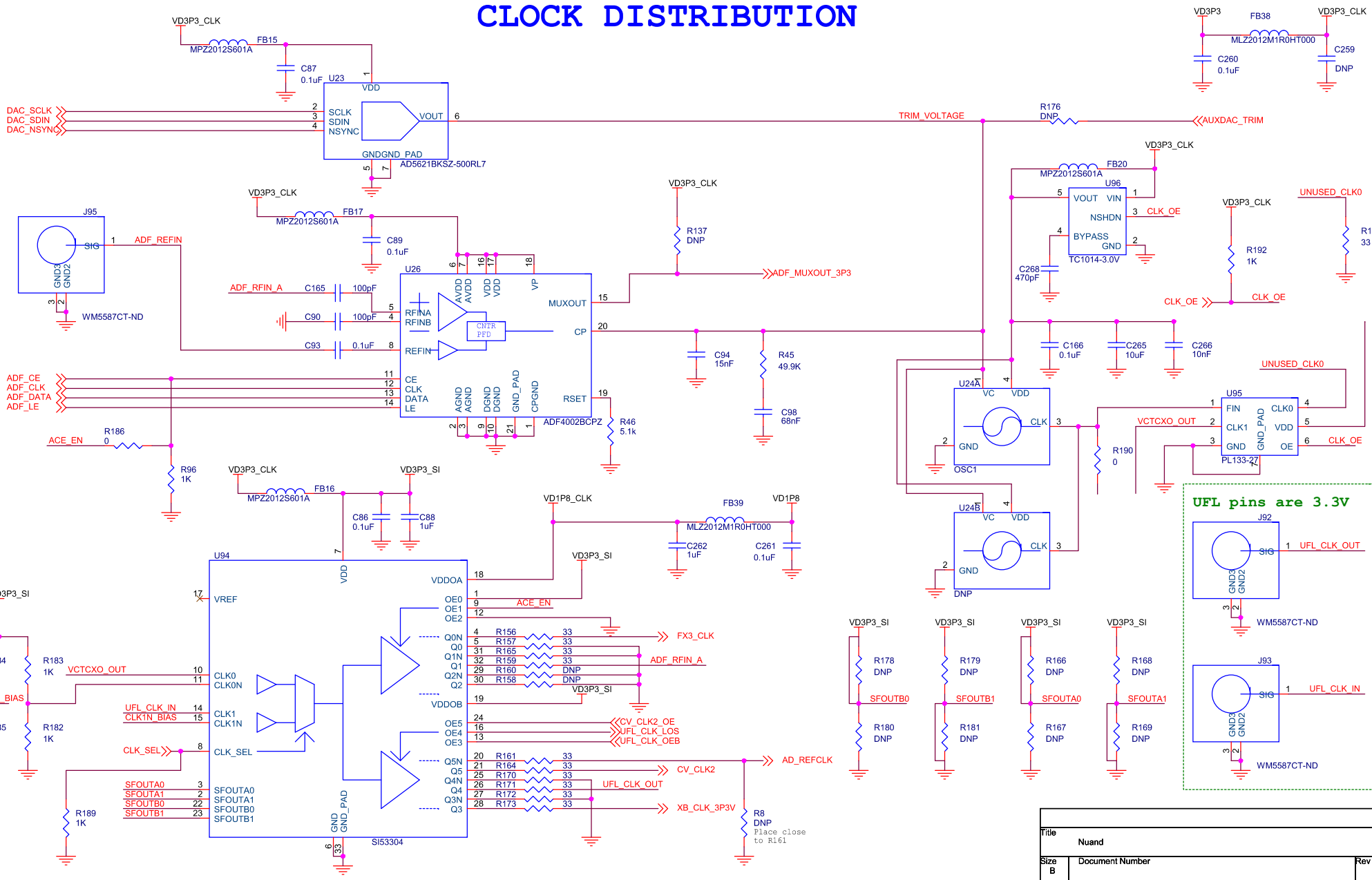
## CVDDQ



- U3RX\_VDDQ = V1P2
- U3TX\_VDDQ = V1P2
- AVDD = V1P2
- CVDDQ = V1P8
- VDD = V1P8
- VIO1 = V1P8
- VIO2 = V1P8
- VIO3 = V1P8
- VIO4 = V3P3
- VIO5 = V1P8

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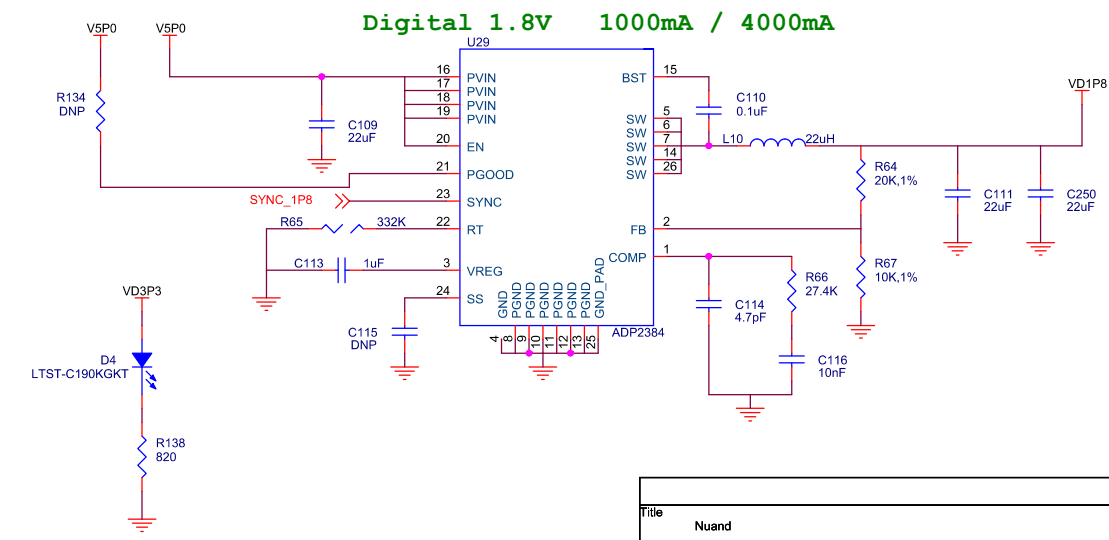
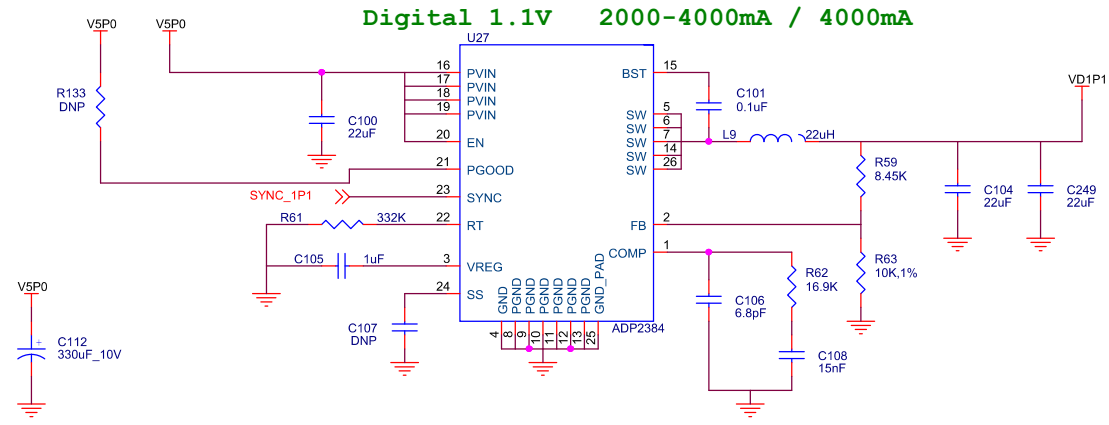
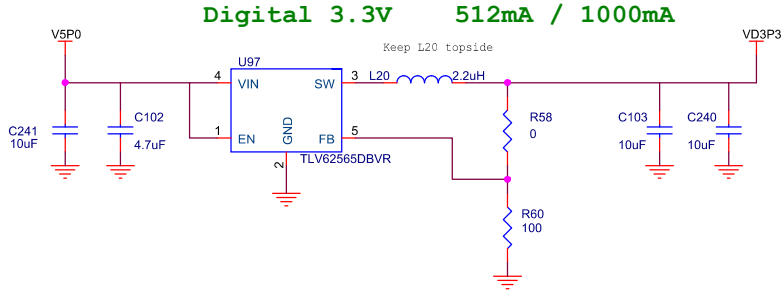
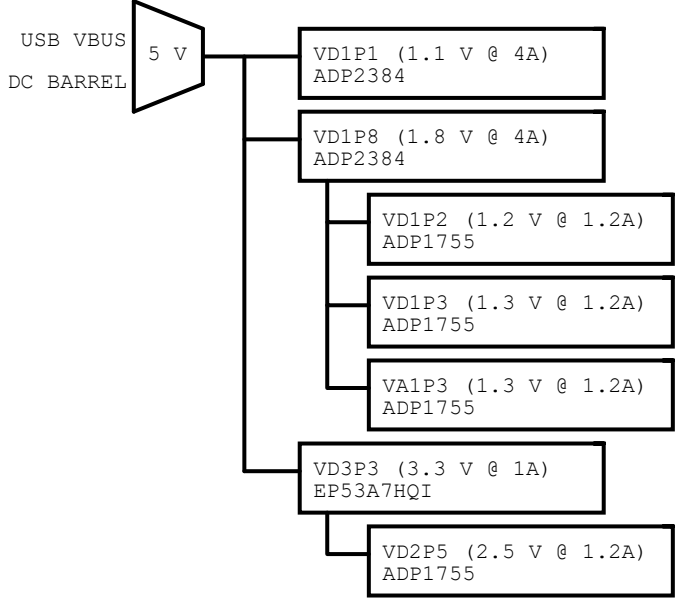
# CLOCK DISTRIBUTION



UFL pins are 3.3V

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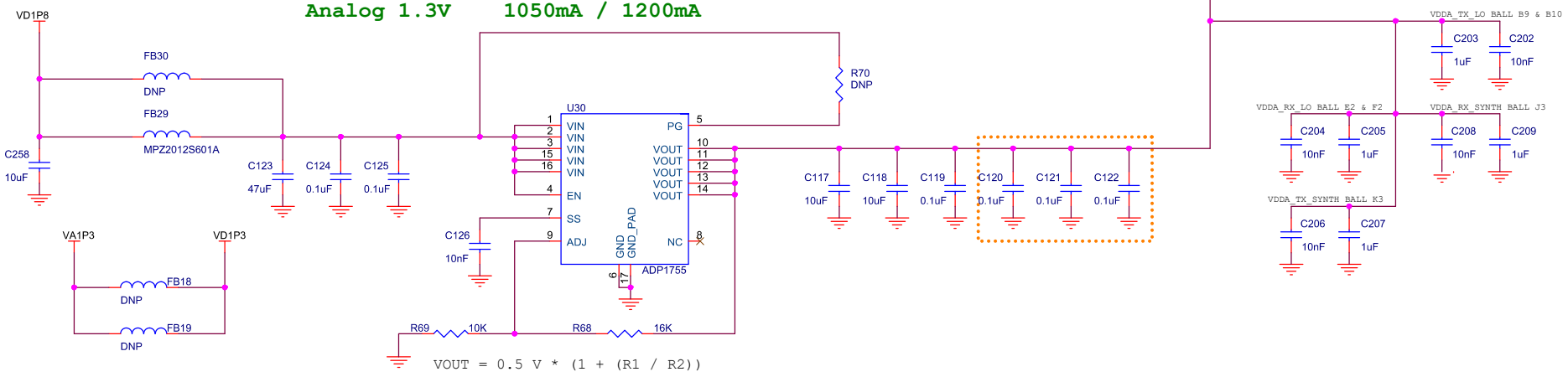
# POWER - 1.1V/1.8V/3.3V



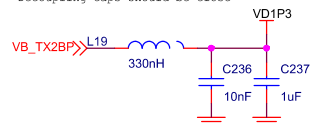
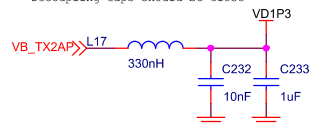
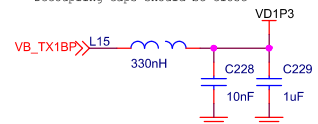
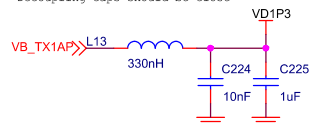
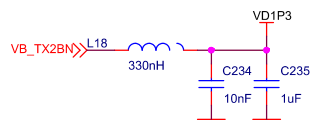
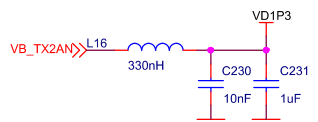
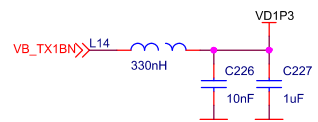
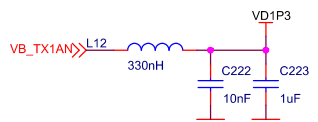
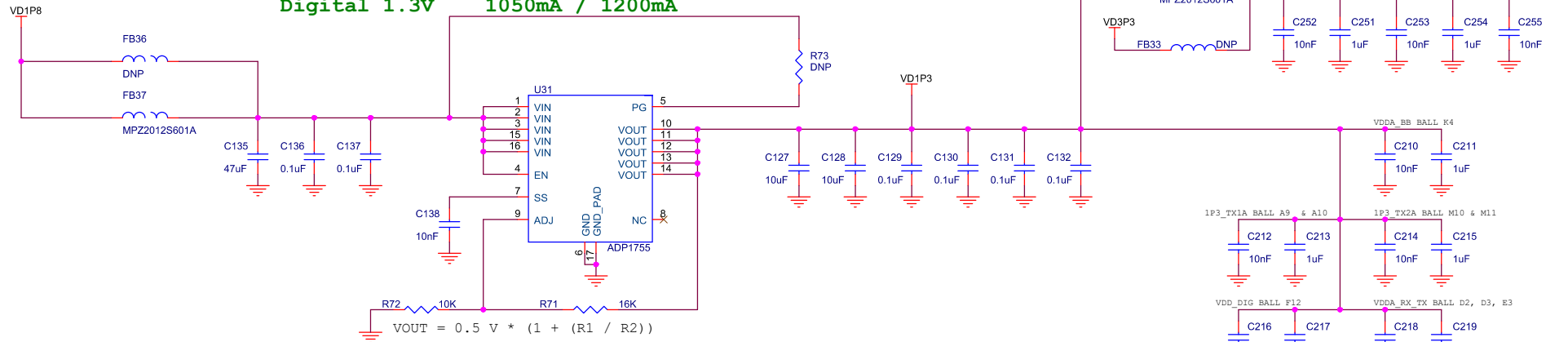
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# POWER - 1.3V

## Analog 1.3V 1050mA / 1200mA



## Digital 1.3V 1050mA / 1200mA



Place inductors inline with RF trace  
Decoupling caps should be close

Place inductors inline with RF trace  
Decoupling caps should be close

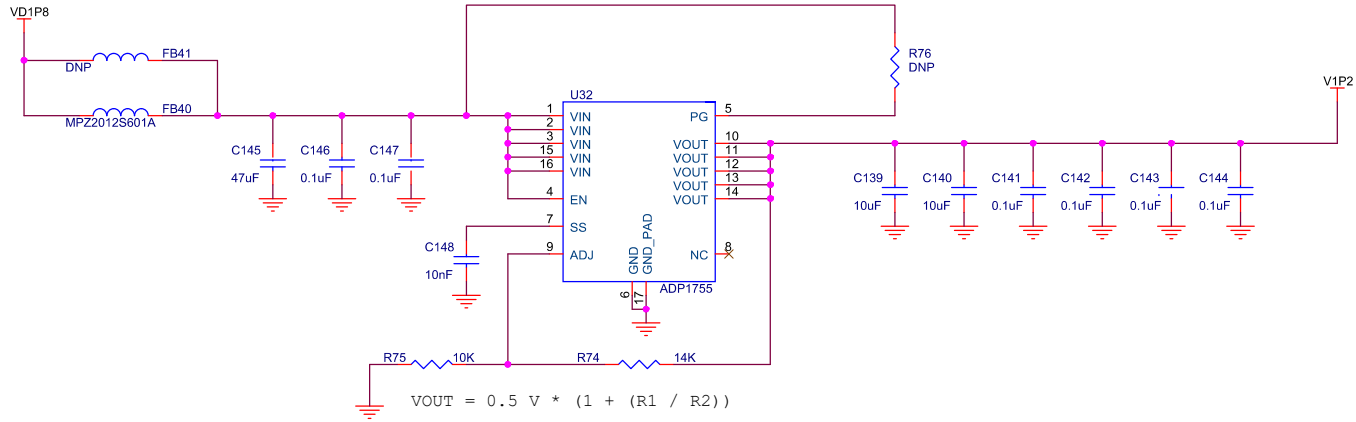
Place inductors inline with RF trace  
Decoupling caps should be close

Place inductors inline with RF trace  
Decoupling caps should be close

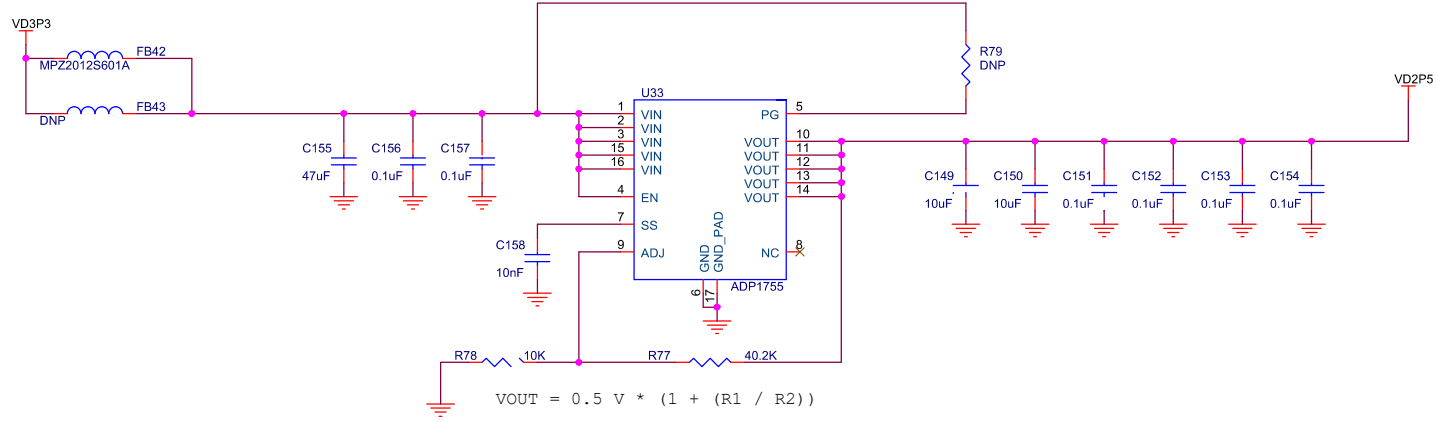
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# POWER - 1.2V/2.5V

Digital 1.2V 197mA / 1200mA



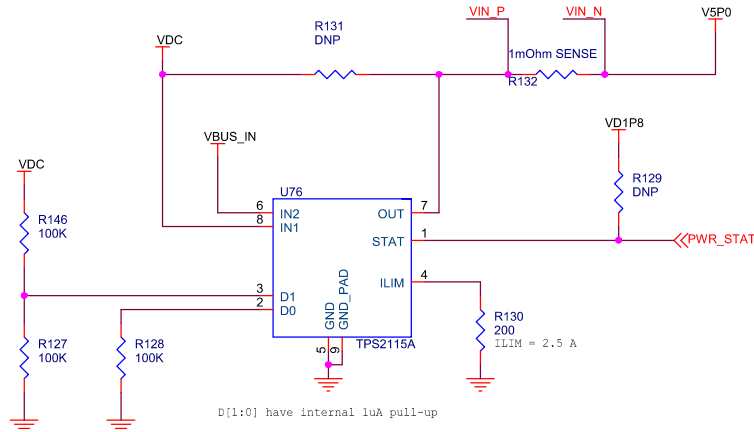
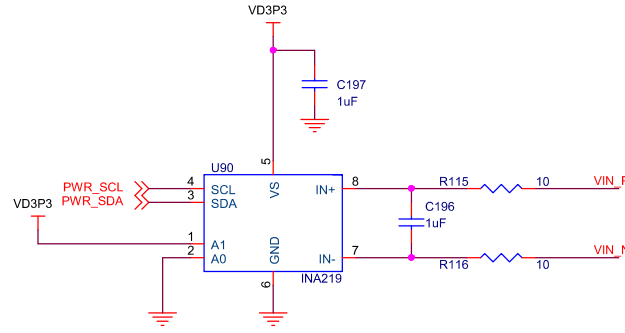
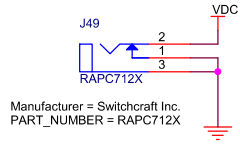
Digital 2.5V 307mA / 1200mA



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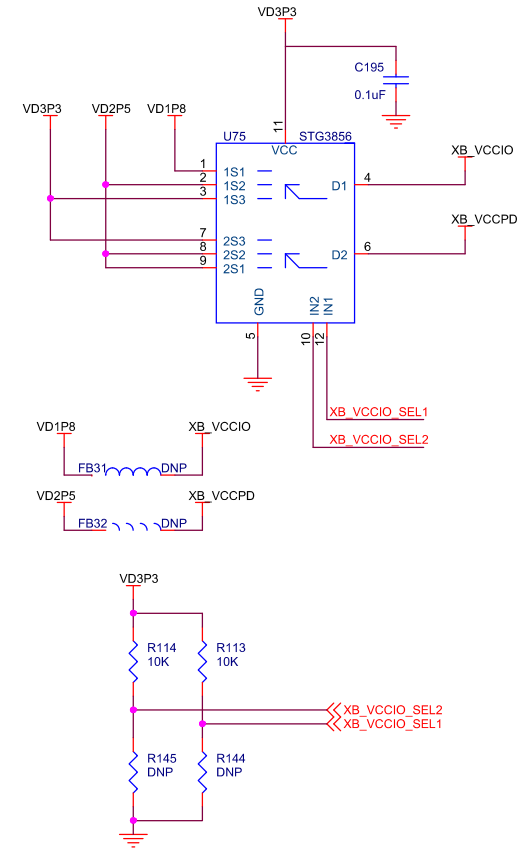
# POWER MUXES AND MONITOR



D1	D0	VIN2 > VIN1	STAT	OUT
<0.7V	<0.7V	X	Z	IN2
>2V	<0.7V	X	0	IN1

If DC barrel jack (VDC) is floating or does not provide at least 4 V, power mux will select USB VBUS.

## XB VCCIO SELECTION



SEL2	SEL1	VCCIO / VCCPD
GND	GND	Hi-Z / Hi-Z
3.3V	GND	1.8 V / 2.5 V
GND	3.3V	2.5 V / 2.5 V
3.3V	3.3V	3.3 V / 3.3 V (DEFAULT)

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